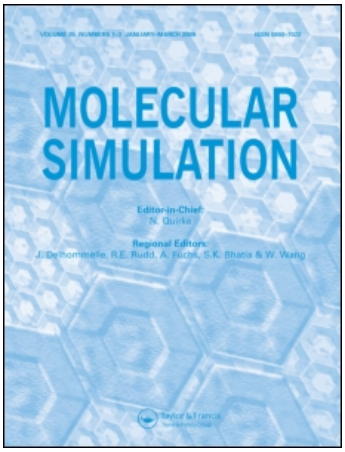

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A continuous surface-potential solution from accumulation to inversion for intrinsic symmetric double-gate MOSFETs

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A continuous surface-potential solution from accumulation to inversion for intrinsic symmetric double-gate MOSFETs

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A continuous surface-potential solution of Poisson's equation is derived for intrinsic (or lightly doped) symmetric double-gate (DG) Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs). The resulting expression is smooth and continuous from accumulation through depletion to inversion regions. The dependences of the surface potential on various physical parameters including the quasi-Fermi potential, silicon film thickness, gate dielectric thickness and temperature are studied and compared with 2-D numerical simulation. Excellent agreements between them suggest that the proposed surface-potential solution is accurate over a wide range of physical parameters and can be used in surface-potential-based symmetric DG MOSFET modelling.

Keywords: non-classical CMOS; surface potential; DG-MOSFETs; device physics; compact modelling; ULSI circuit simulation

1. Introduction

In parallel with the tremendous scaling down of single-gate bulk Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs), all kinds of nanoscale and molecular-level novel devices, including non-classical multiple gate MOSFETs and other molecular electronics, are being extensively studied to extend the geometry shrinking of CMOS into 10 nm generation node and beyond [1]. At the same time, compact models for the emerging novel devices are needed for their circuit application. Recently, surface-potential-based MOSFET models are becoming popular as they provide a more physical description of the molecular-scale MOSFET operation [2–6]. The analysis of surface potential versus gate voltage characteristics of MOS transistor can date back to the 1965 Sah–Pao model [7], which subsequently was used in the Pao–Sah double-integral model to calculate the diffusion and drift drain current [8]. Farrah–Steinberg extended the analysis to double-gate (DG) thin-film transistor [9]. In 2002, a singularity was found in the surface-potential equation near the flat-band voltage [10]. To handle the singularity, some mathematical conditions were proposed [10–11] but the cause of this behaviour remains unresolved [12]. The physical origin of this problem was identified by Sah [13] and He et al. [14] independently and various iterative or analytical solutions [15–19] have been developed following that.

Similar to the single-gate bulk MOSFETs, it is desirable to have a surface-potential-based model for symmetric DG MOSFETs. However, a continuous surface-potential solution that is valid and continuous from accumulation to inversion has not yet been derived. It is because most compact models including potential-, charge- and carrier-based models only account for either electrons or holes singly [20–25], but not both [26–31]. A recent publication addressed the continuity issue by introducing the second carrier type [32], but the continuity of the higher derivatives of the surface potential cannot be guaranteed.

In this work, a continuous and smooth surface-potential model from accumulation to strong inversion is derived for the intrinsic symmetric DG MOSFETs. The accuracy of the model has been verified by comparing with 2-D numerical simulation for various quasi-Fermi potential, temperature, silicon film thickness and gate dielectric thickness.

2. Theoretical derivation

Similar to [24–29], we consider an ideal intrinsic symmetric n-channel MOSFET in which the electrostatics is controlled by the front and back gates. Ignoring short-channel effects for simplicity, the electrostatic in the channel of the DG MOSFETs is described by the 1-D Poisson's equation in the vertical direction given by

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = -\frac{\rho}{\varepsilon_{\mathrm{si}}}. \tag{1}$$

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For an intrinsic symmetric *n*-type DG-MOSFET, we have

$$N_a = N_d = 0. \tag{2}$$

The space charge is simply given by

$$\rho = q(p - n), \tag{3}$$

where electron and hole concentrations can be expressed by the corresponding potential as

$$n = n_i e\left(\frac{q(\phi - V)}{kT}\right), \tag{4}$$

$$p = n_i e\left(-\frac{q(\phi)}{kT}\right), \tag{5}$$

where all the symbols have their usual meanings. Substituting (4) and (5) into (1), the Poisson's equation becomes

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{si}}[e^{(q(\phi - V)/kT)} - e^{-q\phi/kT}] \tag{6}$$

with the symmetric boundary conditions:

$$\begin{aligned} &\frac{d\phi}{dx}(x = 0) = 0, \\ &\frac{d\phi}{dx}\left(x = \pm\frac{T_{si}}{2}\right) = C_{ox}(V_{gs} - \phi_s - \Delta\phi_i) \end{aligned} \tag{7}$$

and

$$\phi\left(x = \pm\frac{T_{si}}{2}\right) = \phi_s, \quad \phi(x = 0) = \phi_0, \tag{8}$$

where ϕ_s and ϕ_0 are the surface potential at the silicon/oxide interface and the potential at the centre of the silicon film.

When a gate voltage larger than the flat-band voltage is applied, electron dominates the channel charge and the hole term is negligible. Thus, (6) can be simplified as

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{(q(\phi - V)/kT)}. \tag{9}$$

The solution of (9) would result in discontinuity near flat-band point, which needs to be corrected. With proper boundary conditions, (9) is analytically solved to give [26,27]

$$\frac{C_{ox}(V_{gs} - \phi_s - \Delta\phi_i)}{\sqrt{2n_i\varepsilon_{si}kT}} = \sqrt{e^{q(\phi_s - V)/kT} - e^{q(\phi_0 - V)/kT}}, \tag{10}$$

$$\phi_s = \phi_0 - \frac{2kT}{q}\ln\cos\left[\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}e^{q(\phi_0 - V)/kT}}\frac{T_{si}}{2}\right]. \tag{11}$$

From Equation (10), we can calculate the potential at the centre of the silicon film:

$$\phi_0 = V + \frac{kT}{q}\ln\left[e^{q(\phi_s - V)/kT} - \frac{C_{ox}^2(V_{gs} - \Delta\phi_i - \phi_s)^2}{2n_i\varepsilon_{si}kT}\right]. \tag{12}$$

Substituting (12) into (11) results in an analytic expression for the surface potential:

$$\frac{C_{ox}(V_{gs} - \Delta\phi_i - \phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}e^{-q(\phi_s - V)/2kT} = \sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}\left[e^{q(\phi_s - V)/kT} - \frac{C_{ox}^2(V_{gs} - \Delta\phi_i - \phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \tag{13}$$

This result is analogous to Equation (15) in [31] but with more explicit dependents on the physical variables. Calculating electric field and potential using (13) can still be discontinuous near the flat-band voltage when the band bending change from negative to positive. The situation is similar to that of bulk MOSFETs [10–14] with an inappropriate simplification on Poisson equation. We would like to point out that the channel potential equations in [26–31] may also result in a similar discontinuity near flat band when the channel potential is less than the thermal voltage.

The discontinuous problem of the DG MOSFET surface potential can be fixed using a similar approach as in bulk MOSFET models by adding a new term $-e^{-(qV/kT)}$ in the right- and left-hand sides of Equation (13) as shown in (14)

$$\frac{C_{ox}(V_{gs} - \Delta\phi_i - \phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}\left[e^{q(\phi_s - V)/kT} - e^{-qV/kT}\right]^{-1/2} = \sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}\left[e^{q(\phi_s - V)/kT} - e^{-qV/kT} - \frac{C_{ox}^2(V_{gs} - \Delta\phi_i - \phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \tag{14}$$

A careful study of (14) shows that the surface potential are continuous through the flat-band points as shown in Figure 1. However, discontinuities still exist for the derivatives of the surface potential as shown in Figure 2. This is similar to the result of [32], in which the inclusion of the hole term fixed the discontinuity in the surface potential but not the higher derivatives.

By more careful consideration of (14) on the mathematical characteristics, a new term $-(q\phi_s/kT)\ e^{-(qV/kT)}$ can cancel the effects of the exponential terms in the derivatives of (14) close to flat band. In such a case, the surface-potential solution

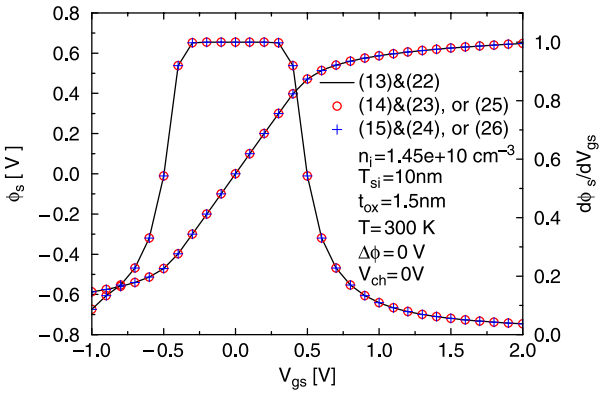

Figure 1. The surface potential and its derivative comparison of a DG MOSFET between three equation pairs for a wide gate voltage range (ϕ_s (left) and $d\phi_s/dV_{gs}$ (right)).

that is infinitely differentiable can be derived and given by

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}\left[e^{q(\phi_s-V)/kT}-\left(1+\frac{q\phi_s}{kT}\right)e^{-qV/kT}\right]^{-1/2} = \sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[e^{q(\phi_s-V)/kT}-\left(1+\frac{q\phi_s}{kT}\right)e^{-qV/kT}-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \quad (15)$$

For the DG-MOSFET operation in the accumulation region, the hole dominates the channel charge. In this case, the derivation of the surface-potential-based on holes is straightforward. Considering only the hole term and ignoring electrons, (6) is simplified to

$$\frac{d^2\phi}{dx^2}=-\frac{qn_i}{\varepsilon_{si}}e^{-q\phi/kT}. \quad (16)$$

Solving (16) gives

$$\frac{C_{ox}(V_{gs}-\phi_s-\Delta\phi_i)}{\sqrt{2n_i\varepsilon_{si}kT}}=-\sqrt{e^{-q\phi_s/kT}-e^{-q\phi_0/kT}}, \quad (17)$$

$$\phi_0-\phi(x)=-\frac{2kT}{q}\ln\cos\left[\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}e^{-q\phi_0/kT}}x\right]. \quad (18)$$

Combining (17) and (18), we have

$$\frac{C_{ox}^2(V_{gs}-\phi_s-\Delta\phi_i)^2}{2n_i\varepsilon_{si}kT}=[e^{-q\phi_s/kT}-e^{-q\phi_0/kT}] \quad (19)$$

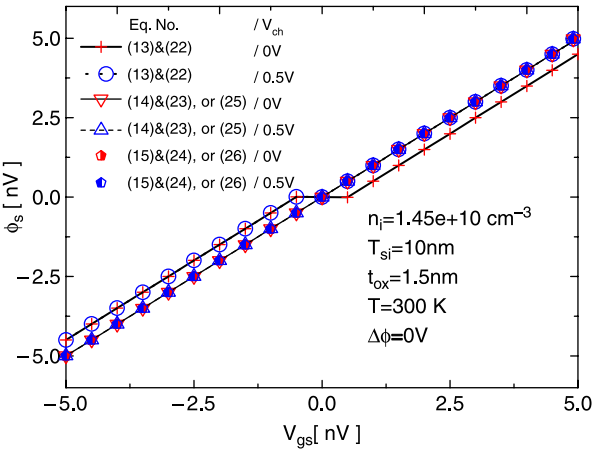

Figure 2. The comparison of ϕ_s versus V_{gs} of near flat band-point between three equation pairs for different V_{ch}, in a refined gate voltage region, showing a discontinuity of the surface potential from Equations (13) and (22) pairs.

and the corresponding surface potential is given by

$$\phi_s=\phi_0+\frac{2kT}{q}\ln\cos\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}e^{-q\phi_0/kT}}\right]. \quad (20)$$

From Equation (20), the potential at the centre of the silicon film can be calculated as

$$\phi_0=-\frac{kT}{q}\ln\left[e^{-q\phi_s/kT}-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]. \quad (21)$$

Substituting (21) into (19) leads to an analytic surface–potential equation in the accumulation region

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}e^{q\phi_s/2kT} = -\sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[e^{-q\phi_s/kT}-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \quad (22)$$

Equation (22) represents the exact solution of the simplified Poisson equation (16) that also has a discontinuity issue near the flat-band point. This discontinuity can fixed by adding a -1 on both sides of the equation

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}[e^{-q\phi_s/kT}-1]^{-1/2} = -\sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[e^{-q\phi_s/kT}-1-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \quad (23)$$

Similar to (14), (23) produces continuous surface potential and field, but the higher derivatives remains

discontinuous near the flat-band. To improve the continuity, a mathematical correction is performed and (23) is modified to

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}\left[e^{-q\phi_s/kT}-1+\frac{q\phi_s}{kT}\right]^{-1/2} = -\sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[e^{-q\phi_s/kT}-1+\frac{q\phi_s}{kT}-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right]. \quad (24)$$

Similar to the case of bulk MOSFETs, a single surface potential versus voltage equation can be obtained for the symmetric DG MOSFETs from the accumulation to strong inversion region using the signum function (sgn) that returns a '1' for depletion and '−1' for accumulation. For example, combining (14) and (23) gives

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}[\theta e^{\mathrm{sgn}(\phi_s)(q\phi_s/kT)}-\theta]^{-1/2} = \mathrm{sgn}(\phi_s) \times \sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[\theta e^{\mathrm{sgn}(\phi_s)(q\phi_s/kT)}-\theta-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right] \quad (25)$$

and combining (15) and (24) gives

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}}\left[\theta e^{\mathrm{sgn}(\phi_s)(q\phi_s/kT)}-\left(1+\mathrm{sgn}(\phi_s)\frac{q\phi_s}{kT}\right)\theta\right]^{-1/2} = \mathrm{sgn}(\phi_s) \times \sin\left[\frac{T_{si}}{2}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}\left[\theta e^{\mathrm{sgn}(\phi_s)(q\phi_s/kT)}-\left(1+\mathrm{sgn}(\phi_s)\frac{q\phi_s}{kT}\right)\theta-\frac{C_{ox}^2(V_{gs}-\Delta\phi_i-\phi_s)^2}{2n_i\varepsilon_{si}kT}\right]}\right], \quad (26)$$

where θ is the effective the quasi-Fermi potential and is given by

$$\theta=\begin{cases} e^{-qV/kT} & \text{above flat-band point} \\ 1 & \text{flat-band or accumulation} \end{cases} \quad (27)$$

Equations (25) and (26) are formulated based on the exact solution of the Poisson's equation from accumulation, through depletion, final to strong inversion region except for signum function term, when the quasi-Fermi potential is zero ($\theta = 1$). This result is similar to that of bulk MOSFET model, where a symmetric surface–potential equation is obtained for both intrinsic and zero quasi-Fermi potential conditions [10–14,19]. However, Equation (25) is continuous for the surface potential and charge while it is not continuous for the surface derivatives and capacitances from the accumulation to the strong inversion region. By contrast, Equation (26) is infinitely continuous for surface potential, charge and all derivatives.

To verify the surface–potential equation, a Newton–Raphson iterative method is used to numerically compare the model and the exact solution of the Poisson's equation. To start the numerical iteration, an initial guess is needed. An inappropriate initial guess for (25) and (26) will result in the incorrect convergence even if when an optimised Newton–Raphson algorithm is used. By carefully studying the implicit Equations (25) and (26), we observed that the silicon film thickness plays a unique role in determining the surface potential. For an infinitely large silicon film thickness, the DG MOSFETs become two intrinsic bulk MOSFETs. Equations (25) and (26) thus become

$$\frac{C_{ox}(V_{gs}-\Delta\phi_i-\phi_s)}{\sqrt{2n_i\varepsilon_{si}kT}} = \mathrm{sgn}(\phi_s)\sqrt{\theta}e^{\mathrm{sgn}(\phi_s)(q\phi_s/2kT)}, \quad (28)$$

where the small $q\phi_s/kT$ and unity terms are ignored (because their effects can only be observed when the operation region is very close to flat-band).

The surface-potential Equation (28) is similar to the solution of the Poisson's equation of intrinsic bulk MOSFETs, and it is the same as that given by Ortiz-Conde et al. [33]. Thus, it has an exact solution based on Lambert W function

$$\phi_s = V_{gs}-\Delta\phi_i - \frac{2kT}{q\,\mathrm{sgn}(\phi_s)}W_0\left[\frac{\sqrt{\theta}}{C_{ox}}\sqrt{\frac{q^2\varepsilon_{si}n_i}{2kT}}e^{\mathrm{sgn}(\phi_s)(q(V_{gs}-\Delta\phi_i)/2kT)}\right]. \quad (29)$$

Using (29) as the initial guess for the iterative solution of (25) and (26) (similar to that being done for the diode in [34]), the numerical Newton–Raphson iterative method can converge into the correct surface-potential value efficiently with a robust and stable routine. The surface potential can then be calculated with different geometry, temperature and biasing voltage.

3. Results and discussion

In the above section, the continuous surface-potential solution for the symmetric DG MOSFETs valid from accumulation to inversion region is proposed. The characteristics of the model are described in this section together with the numerical simulation results.

Figure 1 shows the iterative solution of the surface potential of DG MOSFET and its derivatives as a function of the gate voltage calculated from different equation pairs. In particular, the comparison focuses on three pairs of equations: Equations (13) and (22), Equations (14) and

(23) or Equation (25) and Equations (15) and (24) or Equation (26). Figure 1 plots the calculated ϕ_s (left) and $d\phi_s/dV_{gs}$ (right) versus V_{gs} for a wide range of gate voltages from the three equation pairs. The results from the three equation pairs match very well with such a large gate voltage and we cannot observe any difference from it. This indicates that the modification to Equations (13) and (22) is reasonable and a more refined gate voltage is needed to observe the discontinuity.

Figure 2 shows the calculated ϕ_s versus V_{gs} near flat-band using a more refined gate voltage steps. As shown in Figure 2, Equations (13) and (22) results in a discontinuity of the surface–potential curve. This problem is fixed by adding a $-e^{-(qV/kT)}$ or -1 term to modify Equation (14) or (23) to obtain (25). Surface potential calculated using (25) can pass through the flat-band point smoothly even with zero V_{ch}. Further modification on Equation (25) (i.e. Equation (26)) also demonstrates continuous characteristics in the range from the beyond and above flat-band point region. Moreover, Equation (26) fits the result of (25) so well that there is no observable difference between them. The difference, however, can be observed from the derivatives of Equations (25) and (26) as shown in Figure 3.

Figure 3 plots the numerically calculated of $d\phi_s/dV_{gs}$ from Equations (25) and (26). The surface potential calculated using of Equation (25) shows a discontinuity close to the flat-band point when $V_{ch} \neq 0$. This result indicates that Equation (25) cannot be used to predict the capacitance–voltage characteristics of the DG MOSFETs. Equation (26) fixed the problem and the resulting derivatives of the surface potential is smooth and continuous for $V_{ch} = 0.0$ or 0.5 V as demonstrated in Figure 3.

The continuity of the surface potential and its derivative is a necessary rather than a sufficient condition in model development. To study the accuracy of the model, 2-D numerical simulation is performed and compared with the model prediction from Equation (26). Figure 4 shows the surface potential and silicon film centre potential for different quasi-Fermi potential. The model agrees well with the numerical simulation and the error is $<5\%$. This result is good enough to describe the DG MOSFET behaviour in circuit simulation including distortion analysis and the trans-capacitance calculation.

As in bulk MOSFETs, the DG MOSFETs operate in two very different regions beyond flat band: the sub-threshold region, where the surface potential is almost a linear function of the gate voltage and the strong inversion region, where the surface potential gradually reaches a saturation value. The quasi-Fermi potential only comes into effect when the DG MOSFET operates in the strong inversion region. From Equations (12) and (21), ϕ_0 is calculated from the given ϕ_s, and the result is also shown in Figure 4. ϕ_0 moves together with the surface potential in the sub-threshold region but deviate from each other when the device entered the strong inversion (and also strong accumulation), where it gradually reaches a saturation value. This is due to the logarithmic items in Equations (12) and (21) and the maximum film centric potential can be found to be

$$\phi_{0,\max} = \frac{kT}{q} \ln \theta + \operatorname{sgn}(\phi_s) \frac{kT}{q} \ln \left[\frac{2\pi^2 \varepsilon_{si} kT}{q^2 n_i T_{si}^2} \right]. \qquad (30)$$

Figure 5 shows the comparison of the surface-potential derivatives between the model and the 2-D numerical simulation with different quasi-Fermi potential. The model calculations are continuous, smooth and agree well with the numerical simulation with a maximum error less than 0.1% over a wide range of the quasi-Fermi potential.

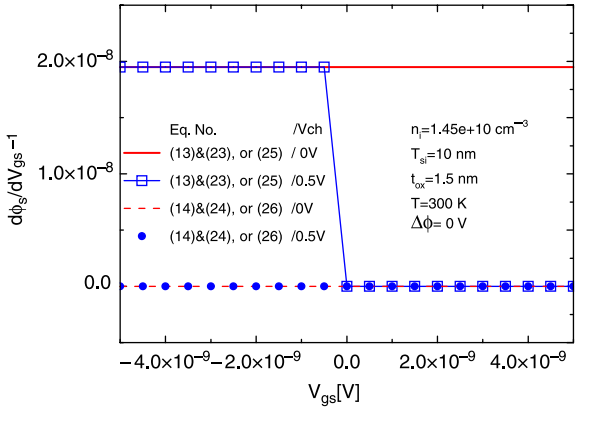

Figure 3. The comparison of $d\phi_s/dV_{gs} - 1$ versus V_{gs} near the flat-band point between Equations (25) and (26), showing the discontinuity of surface-potential derivative from Equation (25) in a DG MOSFET.

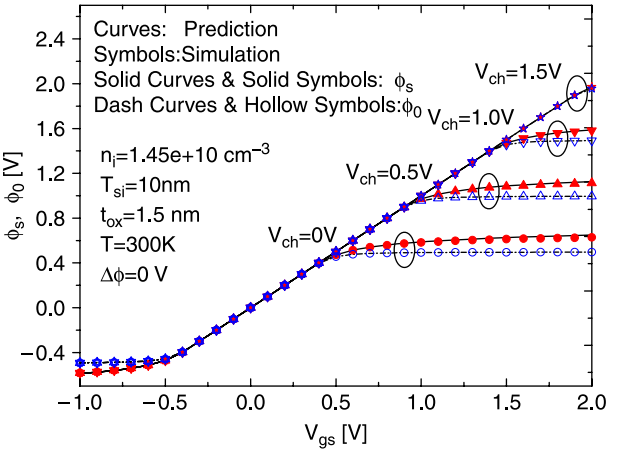

Figure 4. Comparison of ϕ_s and ϕ_0 versus V_{gs} between the 2-D numerical simulation and surface–potential equation prediction for different V_{ch} in a DG MOSFET.

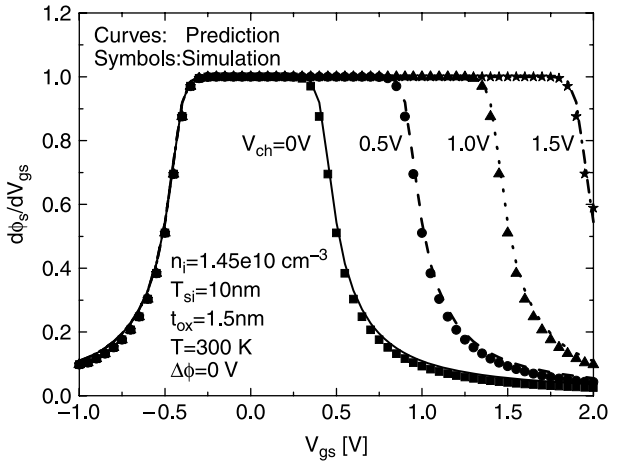

Figure 5. Comparison of the ϕ_s derivatives versus V_{gs} between the 2-D numerical simulation and surface–potential equation prediction for different V_{ch} in a DG MOSFET.

Precise gate capacitance is another desirable feature in the presented surface-potential formulation. Once the surface potential and its derivatives are obtained, the corresponding gate capacitance can be obtained from Equation (10) or (19) by performing the following operation

$$\frac{C_{gg}}{C_{ox}} = \frac{dQ}{C_{ox}dV_{gs}} = 1 - \frac{d\phi_s}{dV_{gs}}. \tag{31}$$

Figure 6 shows the comparison of the gate capacitance calculation from the proposed surface–potential equation and the 2-D numerical simulation with different quasi-Fermi potentials. The predicted gate capacitances are continuous, smooth and agree well with the 2-D numerical simulation.

To further verify the model, comparisons with 2-D numerical simulations for devices with different geometries

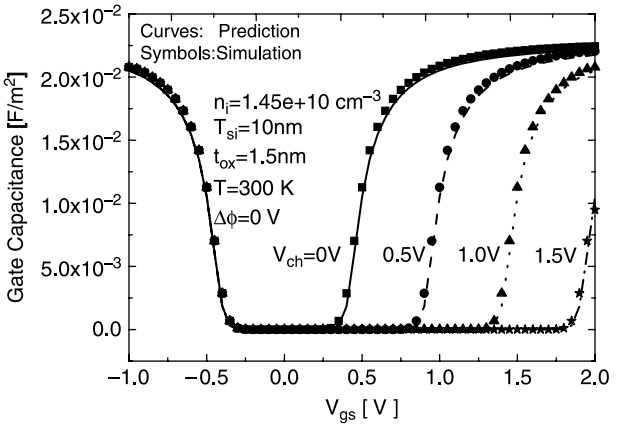

Figure 6. Comparison of the gate capacitance versus V_{gs} between the 2-D numerical simulation and surface–potential equation prediction for different V_{ch} in a DG MOSFET.

operating at different temperatures are performed. Figure 7 shows the surface potential versus gate voltage calculated using the proposed model and the 2-D numeric simulation with different gate oxide thickness. The error between is less than 5%. It is also observed from Figure 7 that a thicker t_{ox} results in a low saturation value and a higher accumulation value of the surface potential, but the film centric potential almost remains constant.

Figure 8 shows the surface potential for devices with different silicon body thickness obtained from the proposed model and 2-D numerical simulation. The results agree very well and the error is less than 0.1%. It is observed from the figure that the effects of silicon body thickness on the surface potential is less obvious, but a general trend of decreasing body centric potential is observed with increasing silicon thickness. This result is the direct consequence of (12) and (21).

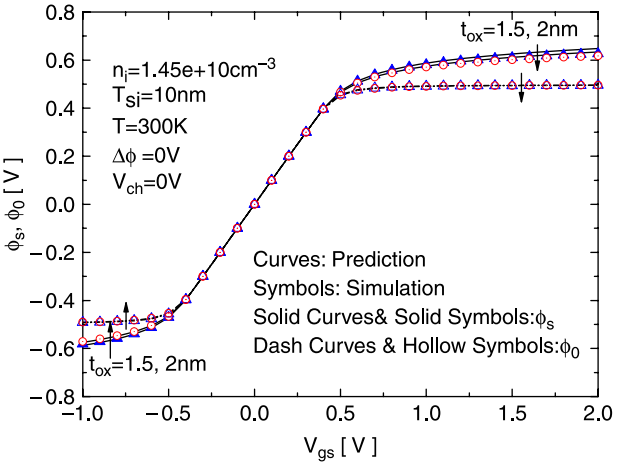

Figure 7. Comparison of ϕ_s and ϕ_0 versus V_{gs} between the 2-D numerical simulation and surface–potential equation prediction for different thickness of gate oxide in a DG MOSFET.

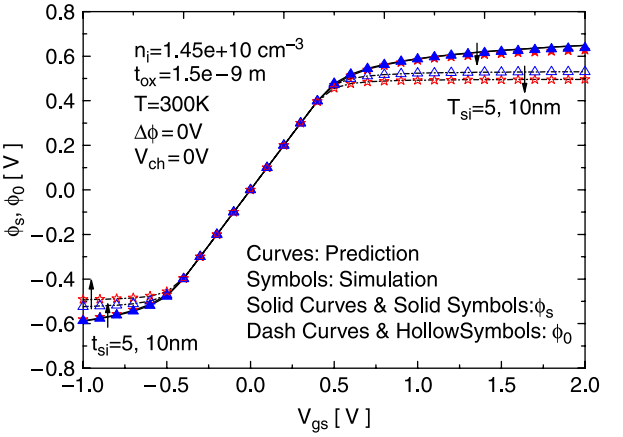

Figure 8. Comparison of ϕ_s and ϕ_0 versus V_{gs} between the 2-D numerical simulation and surface–potential equation prediction for different silicon film thickness in a DG MOSFET.

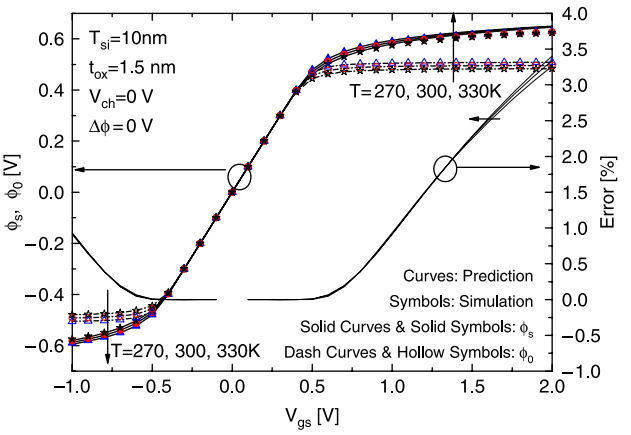

Figure 9. Comparison of ϕ_s and ϕ_0 versus V_{gs} between the 2-D numerical simulation and surface–potential equation and the resultant error of ϕ_s for different operation temperature in a DG MOSFET.

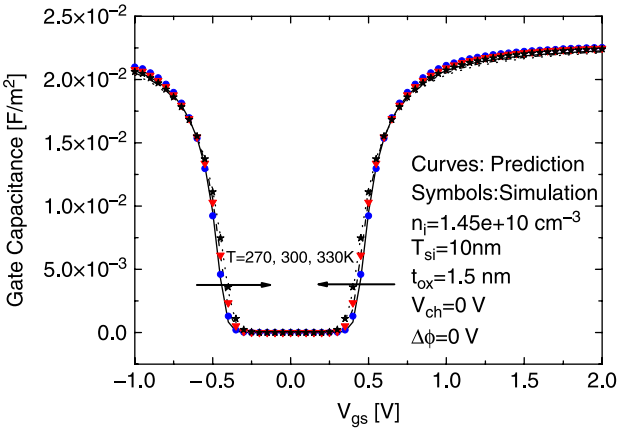

Figure 10. Comparison of the gate capacitance versus gate voltage curves between the 2-D numerical simulation and surface–potential equation prediction for different operation temperature in a DG MOSFET.

Figure 9 shows the surface potential of a DG MOSFET operating at different temperature. Again, the proposed model agrees very well with the 2-D numerical simulation. The absolute value of the surface potential and the body centric potential are larger at higher temperature in both accumulation and strong inversion region. This result is similar to that predicted by the device physics of bulk MOSFETs.

The temperature not only affects the surface potential, but also the gate capacitance. Figure 10 shows the gate capacitance at different temperature obtained from the proposed model and the 2-D numerical simulation. Again, very good agreement is obtained. At a higher temperature, the curves change more smoothly with a lower capacitance value. The curves converge when at very high or low gate voltage corresponding to the strong inversion and the accumulation regions.

4. Conclusions

A smooth and continuous surface-potential model for intrinsic symmetric DG MOSFETs operating from accumulation to strong inversion is proposed in this paper. The continuity and accuracy of the model, including the derivatives, have been extensively verified by 2-D numerical simulation. The result can be used in conjunction with other surface-potential-based models to facilitate the calculation of the surface potential before deriving the I–V equation.

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References

[1] ITRS, *International Technology Roadmap for Semiconductors*, 2007, http://www.itrs.org.
[2] A.R. Boothroyd, S.W. Tarasewicz, and C. Slaby, *MISNAN-A physically based continuous MOSFET model for CAD application*, IEEE Trans. Computer-Aided Design 10(12) (1991), pp. 1512–1528.
[3] HISIM [Online]. Available: http://www.starc.jp/kaihatu/pdgr/hisim/index-e.html.
[4] K. Joardar, K.K. Gullapalli, C.C. McAndrew, M.E. Burnham, and A. Wild, *An improved MOSFET model for circuit simulation*, IEEE Trans. Electron. Dev. 45 (1998), pp. 134–148.
[5] PSP model, http://www.nxp.com/Philips-models/mos_models/psp.
[6] J. He, *Benchmark test on conventional surface potential based charge-sheet models and advanced PUNSIM development*, in *Proceedings of Workshop on Compact Modelling*, 2005, pp. 390–410.
[7] C.T. Sah and H.C. Pao, *The effects of fixed bulk charge on the characteristics of metal–oxide–semiconductor transistor*, IEEE Trans. Electron. Dev. 13(4) (1966), pp. 393–409.
[8] H.C. Pao and C.T. Sah, *Effects of diffusion current on characteristics of metal–oxide (insulator)–semiconductor transistors*, Solid State Electron. 9 (1966), pp. 927–937.
[9] H.R. Farrah and R.F. Steinberg, *Analysis of double-gate thin-film transistor*, IEEE Trans. Electron. Devices 14 (1967), pp. 69–74.
[10] C.C. McAndrew and J. Victory, *Accuracy of approximations in MOSFET charge models*, IEEE Trans. Electron. Dev. 49 (2002), pp. 72–81.
[11] W. Wu, T-L. Chen, G. Gildenblat, and C.C. McAndrew, *Physics-based mathematical conditioning of the MOSFET surface potential equation*, IEEE Trans. Electron. Dev. 51(7) (2004), pp. 1196–1200.
[12] W.Z. Shangguan, M. Saeys, and X. Zhou, *Surface-potential solutions to the Pao–Sah voltage equation*, Solid State Electron. 50(7–8) (2006), pp. 1320–1329.
[13] C.-T. Sah, *A history of MOS transistor compact modelling*, in *Proceedings of Workshop on Compact Modelling*, 2005, pp. 347–390.
[14] J. He, X. Zhang, and Y. Wang, *Comments on 'Modeling MOSFET surface capacitance behavior under non-equilibrium'*, Solid State Electron. 50(2) (2006), pp. 259–262.
[15] T.L. Chen and G. Gildenblat, *Analytical approximation for the MOSFET surface potential*, Solid State Electron. 45 (2001), pp. 335–339.
[16] R.V. Langevelde and F.O.M. Klaassen, *An explicit surface-potential-based MOSFET model for circuit simulation*, Solid State Electron. 44 (2000), pp. 409–418.
[17] M.M. Mattausch, U. Feldmann, A. Rahm, M. Bollu, and D. Savignac, *Unified complete MOSFET model for analysis*

of digital and analog circuits, IEEE Trans. Computer-Aided Design 15 (1996), pp. 1–7.

[18] R. Rios, S. Mudanai, W.-K. Shih, and P. Packan, *An efficient surface potential solution algorithm for compact MOSFET models*, in *Proceedings of International Electron Device Meeting*, 2004, pp. 755–758.

[19] J. He, *A physics-based analytic solution to the MOSFET surface potential from accumulation to strong-inversion region*, IEEE Trans. Electron. Dev. 53(9) (2006), pp. 2008–2016.

[20] Y. Taur, X. Liang, W. Wang, and H. Lu, *A continuous, analytical drain-current model for double-gate MOSFETs*, IEEE Electron. Dev. Lett. 25 (2004), pp. 107–109.

[21] A. Oritiz-Conde, F.J. Garcia Sonchez, and J. Muci, *Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs*, Solid State Electron. 49 (2005), pp. 640–647.

[22] H. Lu and Y. Taur, *An analytic potential model for symmetric and asymmetric DG MOSFETs*, IEEE Trans. Electron. Dev. 53(5) (2006), pp. 1161–1168.

[23] J. He, J. Xi, M. Chan, A.M. Niknejad, and C. Hu, *A non-charge-sheet based analytical model of undoped symmetric double-gate MOSFETs using SPP approach*, in *Proceedings of International Symposium on Quality of Electronic Design*, 2004, pp. 45–50.

[24] A.S. Roy, J.M. Sallese, and C.C. Enz, *A closed-form charge-based expression for drain-current in symmetric and asymmetric double gate MOSFET*, Solid State Electron. 50(4) (2006), pp. 687–693.

[25] J. He, F. Liu, J. Zhang, J. Feng, Y. Song, and M. Chan, *A carrier-based approach for compact modeling of the long channel undoped symmetric double-gate MOSFETs*, IEEE Trans. Electron. Devices 54(5) (2007), pp. 1203–1209.

[26] Y. Taur, *An analytical solution to a double-gate MOSFET with undoped body*, IEEE Electron. Dev. Lett. 21(5) (2000), pp. 245–247.

[27] Y. Taur, *Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFET*, IEEE Trans. Electron. Devices 48(12) (2001), pp. 2861–2869.

[28] A. Oritiz-Conde, F.J. Garcia Sonchez, and S. Malobabic, *Analytic solution of the channel potential in undoped symmetric dual-gate MOSFETs*, IEEE Trans. Electron. Devices 52(7) (2005), pp. 1669–1672.

[29] A. Ortiz-Conde, F.J. García-Sanchéz, J. Muci, and S. Malobabic, *A general analytical solution to the one-dimensional undoped oxide–siliconoxide system*, in *Proceedings of IEEE International Caribean Conference Circuits Devices and Systems*, 2006, pp. 177–182.

[30] X. Shi and M. Wong, *Analytical solutions to the one-dimensional oxide–silicon–oxide system*, IEEE Trans. Electron. Dev. 50 (2003), pp. 1793–1800.

[31] W.Z. Shangguan, X. Zhou, K. Chandrasekaran, Z. Zhu, S.C. Rustagi, S.B. Chiah, and G.H. See, *Surface-potential solution for generic undoped MOSFETs with two gates*, IEEE Trans. Electron. Devices 54(1) (2007), pp. 169–172.

[32] X. Zhou, Z.M. Zhu, S.C. Rustagi, G.H. See, G.J. Zhu, S.H. Lin, C.Q. Wei, and G.H. Lim, *Rigorous surface-potential solution for undoped symmetric double-gate MOSFETs considering both electrons and holes at quasi nonequilibrium*, IEEE Trans. Electron. Devices 55(2) (2008), pp. 616–623.

[33] A. Ortiz-Conde, F.J. Garcia Sanchez, and M. Guzman, *Exact analytical solution of channel surface potential as an explicit function of gate voltage in undoped-body MOSFETs using the Lambert-W function and a threshold voltage definition therefrom*, Solid State Electron. 47(11) (2003), pp. 2067–2074.

[34] J. He, M. Fang, B. Li, and Y. Cao, *A new analytic approximation to general diode equation*, Solid State Electron. 50(8) (2006), pp. 1371–1374.